

# Generated Clocks Demo Script

## Introduction

This demonstration provides high-level instructions on creating constraints for generated clocks and analyzing the timing reports of the generated clock.

### Preparation:

- Required files: \$TRAINING\_PATH/Generated\_Clock/demo/KCU105/verilog
- Required hardware: None

## Generated Clocks

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>• Launch the Vivado™ Design Suite.</li> <li>• Unzip the project using the Tcl Console:  <pre>exec unzip \$::env(TRAINING_PATH) / Generated_Clock/demo/KCU105/verilog.zip -d \$::env(TRAINING_PATH) / Generated_Clock/demo/KCU105/verilog</pre> </li> </ul>	
<ul style="list-style-type: none"> <li>• Open the <b>wave_gen.xpr</b> project from the following directory:  \$TRAINING_PATH/Generated_Clock/demo/KCU105/verilog</li> </ul>	
<ul style="list-style-type: none"> <li>• Open the synthesized design.</li> </ul>	<ul style="list-style-type: none"> <li>• You can open the synthesized design by using either: <ul style="list-style-type: none"> <li>• Flow Navigator</li> <li>• Tcl Console</li> <li>• Horizontal toolbar</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>• Open and view <b>wave_gen_timing.xdc</b>.</li> </ul>	<ul style="list-style-type: none"> <li>• How many clocks are created in the XDC? <ul style="list-style-type: none"> <li>• wave_gen_timing has one created clock constraint on clk_pin_p.</li> </ul> </li> </ul>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Enter <code>report_clocks</code> in the Tcl Console.</li> </ul>	<ul style="list-style-type: none"> <li><code>report_clocks</code> returns a table showing all the clocks in the design.</li> <li>How many clocks are returned from the <code>report_clocks</code> command? <ul style="list-style-type: none"> <li>Four total clocks are returned from the command. You can observe that there are three generated clocks that are propagated from one primary clock.</li> </ul> </li> </ul>
<pre> Clock Report  Attributes P: Propagated G: Generated A: Auto-derived R: Renamed V: Virtual I: Inverted  Clock      Period(ns)  Waveform(ns)  Attributes  Sources clk_pin_p   3.333        {0.000 1.666} P           {clk_pin_p} clkfbout_clk_core  9.999        {0.000 5.000} P,G,A      {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKFBOUT} clk_out1_clk_core  5.000        {0.000 2.500} P,G,A      {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT0} clk_out2_clk_core  5.161        {0.000 2.580} P,G,A      {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT1}  ===== Generated Clocks =====  Generated Clock : clkfbout_clk_core Master Source   : clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKIN1 Master Clock    : clk_pin_p Edges           : {1 2 3} Edge Shifts(ns) : {0.000 3.333 6.666} Generated Sources : {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKFBOUT}  Generated Clock : clk_out1_clk_core Master Source   : clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKIN1 Master Clock    : clk_pin_p Edges           : {1 2 3} Edge Shifts(ns) : {0.000 0.833 1.667} Generated Sources : {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT0}  Generated Clock : clk_out2_clk_core Master Source   : clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKIN1 Master Clock    : clk_pin_p Edges           : {1 2 3} Edge Shifts(ns) : {0.000 0.914 1.828} Generated Sources : {clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT1} </pre>	
<ul style="list-style-type: none"> <li>What are generated clocks? <ul style="list-style-type: none"> <li>Clocks are generated <b>automatically</b> when a primary clock propagates to a cell that generates new clocks.</li> <li>All these clocks can be described in XDC.</li> </ul> </li> </ul>	

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>View the details of the generated clocks in the <code>report_clocks</code> command output.</li> </ul>	<ul style="list-style-type: none"> <li>In addition to the summary of clocks, the <code>report_clocks</code> command shows how each generated clock is generated.</li> <li><b>Master Source</b> is the pin of the clock management cell that receives the input clock.</li> <li><b>Master Clock</b> is the clock that propagated to the Master Source.</li> <li>The relationship between the master and generated clock is shown by: <ul style="list-style-type: none"> <li>Multiply By, Divided By, or Edges, and Edge Shift.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>Let's find out one of the generated clocks by using the master source as a pin.</li> <li>Enter <code>get_clocks -of_objects [get_pins clk_gen_i0/clk_core_i0/inst/mmcm e3_adv_inst/CLKOUT1]</code> in the Tcl console. <ul style="list-style-type: none"> <li>This command returns the generated clock <code>clk_out2_clk_core</code>.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>Clocks generated automatically by the tool are objects.</li> <li>Like all objects, they should be queried by using the available commands.</li> <li>The names of the clocks are not guaranteed to follow any naming convention and may vary between tool versions.</li> <li>The clock should be obtained through an object to which it is attached.</li> </ul>
<ul style="list-style-type: none"> <li>Selecting the path with <code>clk_out2_clk_core</code> as the path group. <ul style="list-style-type: none"> <li>Here you can select any path, one such path is selected here as an example.</li> </ul> </li> <li>Enter <code>report_timing -from [get_pins uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]/C] -to [get_pins uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]/D]</code> in the Tcl console.</li> <li>View the contents of the report.</li> </ul>	<ul style="list-style-type: none"> <li>The requirement used for a path running on a generated clock is determined by the attributes of the generated clock.</li> <li>The clock used for both the source and destination flip-flop is running on the <code>clk_out2_clk_core</code>, which is the output of the MMCM running at 193.75 MHz.</li> </ul>

Action with Description

Point of Emphasis and Key Takeaway

Slack (MET) :4.340ns (required time - arrival time)

Source:uart\_tx\_i0/uart\_baud\_gen\_tx\_i0/internal\_count\_reg[2]/C  
(rising edge-triggered cell FDRE clocked by clk\_out2\_clk\_core (rise@0.000ns fall@2.580ns period=5.161ns))

Destination:uart\_tx\_i0/uart\_baud\_gen\_tx\_i0/internal\_count\_reg[6]/D  
(rising edge-triggered cell FDSE clocked by clk\_out2\_clk\_core (rise@0.000ns fall@2.580ns period=5.161ns))

Path Group:clk\_out2\_clk\_core

Path Type:Setup (Max at Slow Process Corner)

Requirement:5.161ns (clk\_out2\_clk\_core rise@5.161ns - clk\_out2\_clk\_core rise@0.000ns)

Data Path Delay:0.664ns (logic 0.250ns (37.651%) route 0.414ns (62.349%))

Logic Levels:2 (LUT3=1 LUT5=1)

Clock Path Skew:-0.145ns (DCD - SCD + CPR)

Destination Clock Delay (DCD):-1.061ns = ( 4.100 - 5.161 )

Source Clock Delay (SCD):-0.684ns

Clock Pessimism Removal (CPR):0.232ns

Clock Uncertainty:0.071ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE

Total System Jitter (TSJ):0.071ns

Discrete Jitter (DJ):0.122ns

Phase Error (PE):0.000ns

Note: The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

View the source clock path and datapath delay from the report.

Timing reports always start at primary clocks.

Propagates forward to generated clocks, and then on to the clocked elements.

The source clock path starts from clk\_pin\_p and propagates on to mmcm output CLKOUT1; i.e., the generated clock.

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk_out2_clk_core rise edge)				
		0.000	0.000 r	
		0.000	0.000 r	clk_pin_p (IN)
net (fo=0)		0.000	0.000	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/I
DIFFINBUF (Prop_DIFFINBUF_DIFF_IN_P_O)		0.393	0.393 r	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/DIFFINBUF_INST/O
net (fo=1, unplaced)		0.001	0.394	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/OUT
IBUFCTRL (Prop_IBUFCTRL_I_O)		0.000	0.394 r	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/IBUFCTRL_INST/O
net (fo=1, unplaced)		0.785	1.179	clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
MMCM3_ADV (Prop_MMCM3_ADV_CLKIN1_CLKOUT1)		-4.855	-3.676 r	clk_gen_i0/clk_core_i0/inst/mmcm3_adv_inst/CLKOUT1
net (fo=1, unplaced)		0.325	-3.351	clk_gen_i0/clk_core_i0/inst/clk_out2_clk_core
BUFCE (Prop_BUFCE_I_O)		0.083	-3.268 r	clk_gen_i0/clk_core_i0/inst/clkout2_buf/O
net (fo=149, unplaced)		2.584	-0.684	uart_tx_i0/uart_baud_gen_tx_i0/clk
FDRE				uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]/C
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FDRE (Prop_FDRE_C_Q)		0.115	-0.569 r	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]/Q
net (fo=7, unplaced)		0.175	-0.403	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg_n_0[2]
LUT3 (Prop_LUT3_I2_O)		0.395	-0.308 r	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_i_2/O
net (fo=2, unplaced)		0.225	-0.083	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_i_2_n_0
LUT5 (Prop_LUT5_I0_O)		0.040	-0.043 r	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_i_1/O
net (fo=1, unplaced)		0.023	-0.020	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]
FDSE				uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]/D

Note: The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>View the destination clock path timing.</li> </ul>	<ul style="list-style-type: none"> <li>Like other setup checks, the destination clock delay starts at the next clock edge of the primary clock.</li> <li>Propagates to the generated clock and on to the destination flip-flop.</li> <li>The slack is required time – arrival time.</li> <li>Note that a minus sign is added by the tool which may cancel the minus of a negative number.</li> </ul>

(clock clk_out2_clk_core rise edge)			
	5.161	5.161 r	
	0.000	5.161 r	clk_pin_p (IN)
net (fo=0)	0.000	5.161	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/I
DIFFINBUF (Prop_DIFFINBUF_DIFF_IN_P_O)	0.237	5.398 r	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/DIFFINBUF_INST/O
net (fo=1, unplaced)	0.001	5.399	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/OUT
IBUFCTRL (Prop_IBUFCTRL_I_O)	0.000	5.399 r	clk_gen_i0/clk_core_i0/inst/clkin1_ibufds/IBUFCTRL_INST/O
net (fo=1, unplaced)	0.746	6.144	clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
MMCM3_ADV (Prop_MMCM3_ADV_CLKIN1_CLKOUT1)	-4.867	1.277 r	clk_gen_i0/clk_core_i0/inst/mmcm3_adv_inst/CLKOUT1
net (fo=1, unplaced)	0.309	1.586	clk_gen_i0/clk_core_i0/inst/clk_out2_clk_core
BUFGCE (Prop_BUGCE_I_O)	0.075	1.661 r	clk_gen_i0/clk_core_i0/inst/clkout2_buf/O
net (fo=149, unplaced)	2.439	4.100	uart_tx_i0/uart_baud_gen_tx_i0/clk
FDSE		r	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg
clock pessimism	0.232	4.332	
clock uncertainty	-0.071	4.261	
FDSE (Setup_FDSE_C_D)	0.059	4.320	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]
required time		4.320	
arrival time		0.020	
slack		4.340	

- Note:** The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>From the Netlist window, select <b>wave_gen</b> &gt; <b>clk_gen_i0</b> and press &lt;F4&gt; to create a schematic.</li> <li>Click <b>+</b> in <b>clk_gen_i0</b> to expand.</li> <li>Click <b>+</b> in <b>clk_core_i0</b> to expand.</li> <li>Click <b>+</b> in the inst module to expand it.</li> <li>View the design schematic to analyze the logic for <b>clk_samp</b> (CLK).</li> <li>Why should <b>clk_samp</b> (CLK) be constrained?</li> </ul>	<ul style="list-style-type: none"> <li>Examining these above source and destination paths using the schematic.</li> <li>A clock gate (BUFGCE/ BUFHCE) that is enabled periodically generates a decimated clock.</li> <li>The period of the generated clock is N times the period of the input clock if the gate is activated one out of N clocks.</li> <li>The timing engine cannot analyze the structure of the logic generating the CE and hence cannot automatically generate this clock.</li> <li><b>clk_samp</b> (CLK) is an example for this. You have to manually create a constraint for this generated clock.</li> </ul>
<ul style="list-style-type: none"> <li>Enter the following command in the Tcl Console to manually create a constraint:</li> </ul> <pre>create_generated_clock -name clk_samp -source [get_pins {clk_gen_i0/BUFGCE_clk_samp_i0/I }] -divide_by 32 [get_pins {clk_gen_i0/BUFGCE_clk_samp_i0/O }]</pre>	<ul style="list-style-type: none"> <li>The generated clock can be manually generated with the <b>create_generated_clock</b> command.</li> <li><b>create_generated_clock -name &lt;name&gt; -source &lt;source&gt; &lt;relationship&gt; &lt;objects&gt;</b> <ul style="list-style-type: none"> <li><b>&lt;name&gt;</b> is the user-assigned name for the new clock.</li> <li><b>&lt;source&gt;</b> is a port or pin that is associated with the clock to use as the reference clock.</li> <li><b>&lt;relationship&gt;</b> is one of a number of options for specifying the relationship between the source clock and the generated clock.</li> <li><b>&lt;objects&gt;</b> is the list of pins/ports/nets to attach the new clock to.</li> </ul> </li> <li>Save the constraints. You can see the new constraint in <b>wave_gen_timing.xdc</b> to create generated clock <b>clk_samp</b>.</li> </ul>
<ul style="list-style-type: none"> <li>Enter <b>report_clocks</b> in the Tcl Console.</li> </ul>	<ul style="list-style-type: none"> <li>Observe that <b>clk_samp</b> has been added under the generated clocks.</li> </ul>
<ul style="list-style-type: none"> <li>Run the Timing Summary report.</li> </ul>	

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> <li>Select <b>Intra clock paths &gt; clk_samp &gt; setup</b> in the Timing Summary report.</li> <li>Double-click any path under this group (the most critical path, for example) to view its properties.</li> </ul>	<ul style="list-style-type: none"> <li>The source clock delay always starts at the primary clock.</li> <li>Propagates through all generated clocks.</li> <li>In this case, propagates through both an automatically and manually generated clock.</li> <li>The requirement is the period of the manually generated clock.</li> </ul>
<p>The screenshot displays the Vivado Timing Summary report. The 'Summary' section shows the path name 'Path 41' and its slack '162.758ns'. The 'Requirement' is highlighted as '165.145ns (clk_samp rise@165.145ns - clk_samp rise@0.000ns)'. The 'Source Clock Path' section is expanded, showing a table of delays. Red callouts point to specific elements: 'Period of Manually Generated Clock' points to the requirement value; 'Propagation starts at Primary Clock' points to the first row of the Source Clock Path table; 'Automatically Generated Clock' points to the 'clk_gen_i0/clk_core_i0/inst/clkout2_clk_core' resource; and 'Manually Generated Clock' points to the 'smp_gen_i0/smp_cnt_reg[9]/C' resource.</p>	
<ul style="list-style-type: none"> <li><b>Note:</b> The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.</li> </ul>	
<ul style="list-style-type: none"> <li>View the Destination Clock Path section in the Timing Summary report.</li> </ul>	<ul style="list-style-type: none"> <li>Like source clock delay, destination clock delay also starts at the primary clock and propagates through all generated clocks.</li> </ul>

## Action with Description

## Point of Emphasis and Key Takeaway

Destination Clock Path				
Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock clk_samp rise edge)	(r) 165.145	165.145		clk_pin_p
net (fo=0)	(r) 0.000	165.145		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/I
DIFFINBUF		0.000		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/DIFFINBUF_INST/DIFF_IN_P
DIFFINBUF (Prop DIFFINBUF_DIFF_IN_P_O)	(r) 0.237	165.382		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/DIFFINBUF_INST/O
net (fo=1, unplaced)	0.001	165.383		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/OUT
IBUFCTRL		0.000		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/IBUFCTRL_INST/I
IBUFCTRL (Prop IBUFCTRL_I_O)	(r) 0.000	165.383		clk_gen_i0/clk_core_i0/inst/clk_in1_ibufds/IBUFCTRL_INST/O
net (fo=1, unplaced)	0.746	166.128		clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
MMCM3_ADV		0.000		clk_gen_i0/clk_core_i0/inst/mmcm3_adv_inst/CLKIN1
MMCM3_ADV (Prop MMCM3_ADV_CLKIN1_CLKOUT1)	(r) -4.867	161.261		clk_gen_i0/clk_core_i0/inst/mmcm3_adv_inst/CLKOUT1
net (fo=1, unplaced)	0.309	161.570		clk_gen_i0/clk_core_i0/inst/clk_out2_clk_core
BUFCE		0.000		clk_gen_i0/clk_core_i0/inst/clk_out2_buf/I
BUFCE (Prop BUFCE_I_O)	(r) 0.075	161.645		clk_gen_i0/clk_core_i0/inst/clk_out2_buf/O
net (fo=149, unplaced)	2.439	164.084		clk_gen_i0/clk_core_i0/inst/clk_out2_clk_core
BUFCE		0.000		clk_gen_i0/clk_core_i0/inst/clk_out2_buf/I
BUFCE (Prop BUFCE_I_O)	(r) 0.075	164.159		clk_gen_i0/clk_core_i0/inst/clk_out2_buf/O
net (fo=57, unplaced)	2.439	166.598		smp_gen_i0/clk_samp
FDRE		0.000		smp_gen_i0/speed_cnt_reg[14]
clock pessimism	0.385	166.983		
clock uncertainty	-0.071	166.912		
FDRE (Setup FDRE C D)	0.059	166.971		smp_gen_i0/speed_cnt_reg[14]
<b>Required Time</b>		166.971		

Period of Manually Generated Clock

Automatically Generated Clock

Manually Generated Clock

- Note:** The timing numbers may vary depending on the version of the Vivado Design Suite and the OS.

- Close the project and exit the Vivado Design Suite.

## Summary

This demonstration illustrated how to create generated clock constraints and analyze the timing reports of the generated clocks.

### References:

- Supporting materials
  - Vivado Design Suite User Guide: Using Constraints* (UG903)
  - Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906)